REMARKS

It is believed that the above amendments and following remarks attend to each and every rejection and objection presented in the pending October 4, 2005 office action. Claims 1-20 remain pending, with claims 1, 7, 16 and 17 being independent.

Specification

Paragraph [0001] is amended to insert information of related applications as required by paragraph 1 of the pending office action. Paragraph [0028] of the specification is amended to insert the numeral four, which printed badly in the filed copy. No new matter is added. Reconsideration is respectfully requested.

Claim Rejections – 35 U.S.C. §102

Claims 1, 3-7 and 9-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,831,869 granted to Ellis et al. (hereinafter "Ellis"). Respectfully, we disagree.

As way of background, the following summary may help clarify the differences between the immediate application and Ellis. The immediate application teaches of a method, system and software product for utilizing results of a fast analysis of a circuit design during a detailed analysis of the circuit design. A fast analysis of a circuit design may analyze one or more blocks without tracing hierarchical information, whereas a detailed analysis traces nets of each block using hierarchical information. Therefore, during the fast analysis, assumptions of signal nets ported from each block are made to allow results to be quickly determined. During the detailed analysis of the circuit design, if the hierarchical signal net connectivity of block instances within the circuit design matches the assumptions used during the fast analysis of the block, the fast analysis results are utilized to generate detailed analysis results; otherwise, the instance of the block is analyzed to determine the detailed analysis results. Thus, the detailed analysis run time may be shortened if the fast analysis results are used during the detailed analysis.

On the other hand, Ellis discloses a process of compacting or "Flattening" a hierarchical multi-level logic design for more efficient timing. See Ellis abstract. Ellis makes no disclosure of reusing results from one analysis within a second analysis.

Ellis is very different from the claims of the immediate application. For example, as shown in the flowchart of FIG. 5, Ellis reads connectivity information for lower level logic design, creates a new design file for the lower level logic design, analyzes the lower level logic design (steps 106-110) and then deletes internal circuitry of the lower level logic design within the created design file. More specifically, for each lower level logic design, Ellis removes 'internal nets' and retains the nets and delay information contained in logic paths running between the logic design's state devices (e.g., flip-flops) to external connectors. Then, when processing the higher level logic design, Ellis creates a design file for the higher level logic design and substitutes the created lower level logic design files for each lower level logic design within the higher level design file before performing an analysis of the higher level logic design. In effect, Ellis replaces the lower level logic designs with simplified designs to reduce analysis effort and file size. Ellis does not disclose using fast analysis results within a detailed analysis of a circuit design, as taught by the immediate application. The process of Ellis discloses only a static timing analysis. See Ellis col. 4, lines 1-5. Ellis, in fact, performs this timing analysis on both high level logic design and lower level logic design, unlike the immediate application, which may use results from a fast analysis of the circuit design during a detailed analysis of the circuit design.

To anticipate a claim, Ellis must teach every element of the claim and "the identical invention must be shown in as complete detail as contained in the ... claim." MPEP 2131 citing Verdegaal Bros. V. Union Oil Co. of California, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) and Richardson v. Suzuki Motor Co., 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989). Ellis does not teach every element of claims 1, 3-7 and 9-20.

Claim 1 recites a method for utilizing fast analysis information during detailed analysis of a circuit design, including:

a) electronically analyzing one or more design blocks of the circuit design to determine fast analysis results based upon one or more assumptions of ported signal nets of each one of the design blocks;

b) determining whether hierarchical signal net connectivity of block instances of the design blocks matches the assumptions;

c) if the hierarchical signal net connectivity matches the assumptions, utilizing the fast analysis results to generate detailed analysis results; and

d) if the hierarchical signal net connectivity does not match the assumptions, electronically analyzing the one or more blocks to generate detailed analysis results.

As shown in FIG. 5, Ellis discloses that a static timing analysis is performed on each lower level logic design (step 110) and that a static timing analysis is performed on higher level logic design (step 126). Thus, Ellis performs the same analysis on lower level logic design as upper level logic design. Clearly, Ellis does not disclose a fast analysis and a detailed analysis. Step a) of claim 1 requires that one or more design blocks of the circuit design be electronically analyzed to determine fast analysis results based upon one or more assumptions of ported signal nets of each one of the design blocks. Since Ellis does not disclose determining fast analysis results, Ellis cannot determine fast analysis results as required by step a). Further, Ellis does not disclose making assumptions of ported signal nets when analyzing the one or more blocks. In paragraph 3 of the pending office action, the Examiner asserts that Ellis, in FIGs. 10, 11, 14 and 17, col. 12, lines 19-48 and col. 13, lines 51-62 anticipates step b) of claim 1. However, Ellis does not disclose use of assumptions during analysis of lower level logic; it therefore cannot determine whether hierarchical signal net connectivity of block instances of the design blocks matches the assumptions, as required by step b) of claim 1. Since Ellis does not determine fast analysis results as required by step a), Ellis cannot utilize the fast analysis results to generate detailed analysis results if the hierarchical signal net connectivity matches the assumptions, as required by step c). Step d) requires that detailed analysis results be generated by analyzing the block if the hierarchical signal net connectivity does not match the assumptions. However, since Ellis excludes internal nets of lower level logic design, Ellis cannot perform a detailed analysis to produce detailed results.

For at least these reasons, Ellis cannot anticipate claim 1. Reconsideration of claim 1 is respectfully requested.

Claims 3-6 depend from claim 1 and benefit from like argument. However, these claims have additional features that patentably distinguish over Ellis. For

example, in claim 3, assumptions specify that ported signal nets do not connect to power nets. Although the Examiner correctly states that FIGs. 8 and 9 of Ellis do not show power nets, Ellis also does not disclose that any assumption is made about power net connectivity. In fact, Ellis does not even mention power nets or their connectivity. The fact that power nets are not shown in a figure does not indicate that Ellis purposefully excluded them.

More particularly, in paragraph [0033] of the immediate application, "fast analysis tool 124 'assumes' that port 32 (and hence 'ported' signal net 20) connects to another signal net (as opposed to a power net) external to block D." Ellis, on the other hand, discloses no similar assumption.

Claim 4 recites that the assumptions specify that a ported signal net connected to a first FET within a design block also connects to a signal net connected to a second FET external to the design block, and that the second FET is of the opposite type to the first FET. Ellis does not show or mention – anywhere – FETs or transistors. Therefore, Ellis cannot disclose assumptions regarding FET connectivity. In fact, as argued above, Ellis makes no disclosure regarding any connectivity assumptions.

Claim 5 recites generating assumption information defining which assumptions were utilized in determining the fast analysis results. Ellis does not generate assumption information defining which assumptions were utilized in determining the fast analysis results. For example, Ellis does not generate fast analysis results; it also does not disclose that assumptions are made, and again does not generate assumption information.

Claim 6 recites reading instantiation characteristics to determine the block instances. Ellis traces forward paths from a lower level design's non-scan primary data input pins to the first level of state devices and marks instances encountered along the way. See, for example, Ellis col. 10, lines 54-60. However, Ellis does not disclose reading instantiation characteristics to determine block instances.

For at least these reasons, claims 3-6 cannot be anticipated by Ellis. Reconsideration of claims 3-6 is respectfully requested.

Claim 7 recites a system for utilizing fast analysis information during detailed analysis of a circuit design, including:

a) a fast analysis tool for electronically analyzing one or more design blocks of the circuit design to determine fast analysis results based upon assumptions of ported signal nets of each one of the design blocks; and

b) a detailed analysis tool for determining whether hierarchical signal net connectivity of block instances of the design blocks matches the assumptions, the detailed analysis tool utilizing the fast analysis results to generate detailed analysis results when the hierarchical connectivity matches the assumptions and electronically analyzing instances of the one or more blocks to generate detailed analysis results when the hierarchical connectivity does not match the assumptions.

As argued above, Ellis does not disclose both a fast analysis tool, as required by element a) of claim 7, and a detail analysis tool, as required by element b). Ellis certainly does not disclose or suggest determining fast analysis results based upon assumptions of ported signal nets of each one of the design blocks, as required by element a). Since Ellis does not make assumptions, Ellis cannot determine if hierarchical signal net connectivity of block instances of the design blocks matches the assumptions made by the fast analysis tool. Ellis also excludes internal nets of lower level logic design, thus making detailed analysis (as required by element b) impossible.

For at least these reasons, Ellis cannot anticipate claim 7. Reconsideration of claim 7 is respectfully requested.

Claims 9-15 depend from claim 7 and benefit from like argument. However, these claims have additional features that patentably distinguish over Ellis. For example, claim 9 recites that the assumptions specify that the ported signal nets do not connect to power nets. As argued above, Ellis does not disclose any assumption about power net connectivity. In fact, Ellis does not mention power nets or their connectivity.

Claim 10 recites that the assumptions specify that a ported signal net connected to a first FET within a design block also connects to a signal net connected

to a second FET external to the design block and that the second FET is of the opposite type to the first FET. Again, Ellis does not show or mention FETs or transistors, nor does it disclose assumptions regarding FET connectivity.

Claim 11 recites that the fast analysis tool generates assumption information defining which assumptions were utilized in determining the fast analysis results. Ellis does not generate assumption information defining which assumptions were utilized in determining the fast analysis results. Again, Ellis does not disclose generating fast analysis results, and then clearly does not disclose use of assumptions during a fast analysis.

Claim 12 recites that the detailed analysis tool reads instantiation characteristics to determine block instances. As argued above, Ellis does not disclose reading instantiation characteristics to determine block instances.

Claim 13 recites a database for storing fast analysis results for access by the detailed analysis tool. Ellis does not generate fast analysis results and cannot therefore store these results in a database for access by a detailed analysis tool.

Claim 14 recites that the database stores the assumptions. Ellis does not disclose assumptions nor storing assumptions in the database.

Claim 15 recites that the database stores the detailed analysis results. Ellis makes no disclosure of storing results in a database.

For at least these reasons, Ellis cannot anticipate claims 8-15. Reconsideration of claims 8-15 is respectfully requested.

Claim 16 recites a system for utilizing fast analysis information during detailed analysis of a circuit design, including:

a) means for electronically analyzing one or more design blocks of the circuit design to determine fast analysis results based upon assumptions of ported signal nets of each one of the design blocks;

b) means for determining whether hierarchical signal net connectivity of block instances of the design blocks matches the assumptions;

c) means for utilizing the fast analysis results to generate detailed analysis results when the hierarchical signal net connectivity matches the assumptions; and

d) means for electronically analyzing the one or more blocks to generate detailed analysis results when the hierarchical signal net connectivity does not match the assumptions.

Again, Ellis performs the same analysis on lower level logic design as upper level logic design and does not disclose a fast analysis and a detailed analysis. Since Ellis does not disclose determining fast analysis results, Ellis cannot anticipate step a). Further, Ellis does not disclose making assumptions of ported signal nets when analyzing the one or more blocks, and therefore Ellis cannot determine whether hierarchical signal net connectivity of block instances of the design blocks matches the assumptions, as required by step b). Again, since Ellis does not determine fast analysis results as required by step a), Ellis cannot utilize the fast analysis results to generate detailed analysis results if the hierarchical signal net connectivity matches the assumptions, as required by step c). Because Ellis excludes internal nets of lower level logic design, Ellis cannot perform an analysis to produce detailed results as required by step d).

For at least these reasons, Ellis cannot anticipate claim 16. Reconsideration of claim 16 is respectfully requested.

Claim 17 recites a software product with instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for utilizing fast analysis information during detailed analysis of a circuit design, including:

a) instructions for electronically analyzing one or more design blocks of the circuit design to determine fast analysis results based upon assumptions of ported signal nets of each one of the design blocks;

b) instructions for determining whether hierarchical signal net connectivity of block instances of the design blocks matches the assumptions;

c) instructions for utilizing the fast analysis results to generate detailed analysis results when the hierarchical signal net connectivity matches the assumptions; and

d) instructions for electronically analyzing the one or more blocks to generate detailed analysis results when the hierarchical signal net connectivity does not match the assumptions.

Again, Ellis does not disclose determining fast analysis results, and therefore cannot anticipate step a) of claim 17. Ellis also cannot utilize the fast analysis results to generate detailed analysis results if the hierarchical signal net connectivity matches the assumptions, as required by step c). Since, Ellis does not disclose making assumptions of ported signal nets when analyzing the one or more blocks, Ellis cannot determine whether hierarchical signal net connectivity of block instances of the design blocks matches the assumptions, as required by step b). Thus, Ellis cannot perform an analysis to produce detailed results as required by step d), since Ellis excludes internal nets of lower level logic design.

For at least these reasons, Ellis cannot anticipate claim 17. Reconsideration of claim 17 is respectfully requested.

Claims 18-20 depend from claim 17 and benefit from like argument. However, these claims have additional features that patentably distinguish over Ellis. For example, claim 18 recites that the assumptions specify that (a) the ported signal nets do not connect to power nets and (b) a ported signal net connected to a first FET within a design block also connects to a signal net connected to a second FET external to the design block, and that the second FET is of the opposite type to the first FET. As argued above, Ellis does not mention FETs or transistors, and therefore cannot disclose assumptions regarding FET connectivity. Again, Ellis makes no disclosure regarding connectivity assumptions. Claim 19 recites generating assumption information defining which assumptions were utilized in determining the fast analysis results. Again, Ellis does not generate assumption information defining which assumptions were utilized in determining fast analysis results. Ellis does not disclose that assumptions are made during analysis, and therefore cannot generate assumption information. Claim 20 recites reading instantiation characteristics to determine the

block instances. Ellis simply does not disclose reading instantiation characteristics to determine block instances.

For at least these reasons, claims 18-20 cannot be anticipated by Ellis. Reconsideration of claims 18-20 is respectfully requested.

Claim Rejections – 35 U.S.C. §103

Claims 2 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ellis in view of Publication No. US 2002/0002701 A1 (hereinafter, "Usami"). Respectfully we disagree.

When applying 35 U.S.C. §103, the following tenets of patent law must be adhered to:

a) The claimed invention must be considered as a whole;
b) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
c) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and
d) Reasonable expectation of success is the standard with which obviousness is determined. MPEP §2141.01, *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1134 n.5, 229 U.S.P.Q. 182, 187 n.5 (Fed. Cir. 1986).

In addition, it is respectfully noted that to substantiate a *prima facie* case of obviousness the initial burden rests with the Examiner who must fulfill three requirements. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. (emphasis and formatting added) MPEP § 2143, *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

Usami discloses a method and apparatus for automatic circuit generation. In particular, Usami concerns replacing cells (blocks) of a circuit design with new cells to reduce standby leakage current. Usami inputs circuit information, then identifies a path whose delay time is later than a timing constraint, and then replaces high-threshold cells in at least part of the path whose delay time is larger than the timing constraint. Usami does not disclose or suggest utilizing results from a fast analysis within a detailed analysis of a circuit design.

Claim 2 depends from claim 1 and recites that the fast analysis results and detailed analysis results include FET leakage current. Usami determines static timing results but does not perform a fast analysis or make assumptions about hierarchical connectivity. Further, Usami does not utilize fast analysis results based upon assumptions made during the fast analysis. Therefore, Usami does not overcome the shortfall of Ellis in anticipating claim 1. Further, since claim 2 requires that both fast analysis results and detailed analysis results include FET leakage current, Usami cannot anticipate claim 2, since Usami does not disclose both a fast analysis and a detailed analysis results. Thus, even when combined, Ellis and Usami cannot render claim 2 obvious.

Reconsideration of claim 2 is respectfully requested.

Claim 8 depends from claim 7 and recites that the fast analysis results and detailed analysis results include FET leakage current. Usami does not overcome the shortfall of Ellis in anticipating claim 7. In particular, Usami does not disclose fast analysis results and detained analysis results and, thus, even when combined, Ellis and Usami cannot render claim 8 obvious.

Reconsideration of claim 8 is respectfully requested.

In view of the above amendments and arguments, we respectfully request reconsideration and solicit a notice of allowance for claims 1-20.

It is believed that no fees are due in connection with this amendment. If any fee is due, please charge Deposit Account No. 08-2025.

Respectfully submitted,

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